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Date: November 16, 2005 Name: Joseph W. Fleralge Signature:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	Chandrasekharan Kothandaraman, et al.
Appln. No.:	10/769,101
Filed:	January 29, 2004
For:	SINGLE-POLY 2-TRANSISTOR BASED FUSED ELEMENT
Attorney Docket No:	2002 P 03440 US (BHGL No. 10808/138)

Examiner: WILSON, ALLAN R.
Art Unit: 2815

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL

Sir:

Attached is/are:

☒ Transmittal Letter: Response and Amendment Pursuant to 37 C.F.R. §1.116
☐ Return Receipt Postcard

Fee calculation:

☒ No additional fee is required.
☐ Small Entity.
☐ An extension fee in an amount of $_____ for a _____-month extension of time under 37 C.F.R. § 1.136(a).
☐ A petition or processing fee in an amount of $_____ under 37 C.F.R. § 1.17(_____).
☐ An additional filing fee has been calculated as shown below:

					Small Entity			Not a Small Entity	
	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Rate	Add'l Fee	or	Rate	Add'l Fee
Total		Minus			x $25=			x $50=	
Indep.		Minus			x 100=			x $200=	
First Presentation of Multiple Dep. Claim					+$180=			+ $360=	
					Total	$		Total	$

Fee payment:

☐ A check in the amount of $_____ is enclosed.
☐ Please charge Deposit Account No. 23-1925 in the amount of $. A copy of this Transmittal is enclosed for this purpose.
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☒ The Director is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this paper (including any extension fee required to ensure that this paper is timely filed), or to credit any overpayment, to Deposit Account No. 23-1925.

November 16, 2005
Date

Respectfully submitted,

Joseph W. Fleralge (Reg. No. 52,897)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being sent via facsimile to **Examiner Eckert** at 571-273-8300 at the United States Patent Office, on:

November 16, 2005
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Joseph W. Flerlage, Reg. No. 52,897
Name of Registered Representative

Signature

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Reference No. 2002 P 03440 US
Our Case No. 10808/138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Chandrasekharan Kothandaraman, *et al.*	
Serial No.: 10/769,101	Examiner ECKERT II, George C.
Filing Date: January 29, 2004	Group Art Unit No. 2815
For SINGLE-POLY 2-TRANSISTOR BASED FUSE ELEMENT	

RESPONSE AND AMENDMENT PURSUANT TO 37 C.F.R. § 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed on September 19, 2005, Applicants respectfully request favorable consideration in light of the following:

Amendments to the Claims are reflected in the listing of claims which begin on page 2.

Amendments to the Drawings begin on page 6 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks begin on page 7 of this paper.

An **Appendix** including formal drawings is attached following page 9 of this paper.

Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims.

Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims.

1. (Currently Amended) An electrically programmable transistor fuse having a substrate of semiconductor material of a first conductivity type, a source region and drain region disposed in said substrate and spaced apart to define a substantially continuous channel region of monolithic substrate material therebetween, and a layer of insulating material having a uniform thickness and disposed over said source region, drain region and channel region, said electrically programmable transistor fuse comprising:

a first gate and a second gate disposed in a single layer of polysilicon over said insulating material, said first gate disposed overlapping a portion of said source region and said second gate electrically isolated from said first gate and disposed overlapping a portion of said drain region, wherein said first gate includes a terminal for receiving an externally applied signal and said second gate is capacitively coupled to said drain region; and

a coupling device disposed within said substrate and adapted to increase capacitive coupling of said second gate and said drain region, wherein programming is effectuated by charging said second gate via capacitive coupling with said drain region.

2. (Original) The fuse of Claim 1, wherein said programming is effectuated via application of a voltage signal to said drain region and said voltage signal is less than junction breakdown of said transistor fuse.

3. (Original) The fuse of Claim 1 further comprising an extended width drain portion integral with said drain region disposed in said substrate overlapping said second gate for increasing capacitive coupling.

4. (Original) The fuse of Claim 1 further comprising an extended width drain portion integral with said drain region disposed in said substrate overlapping a portion of said second gate and a well region disposed in said substrate also overlapping a portion of said second gate, wherein said well region is isolated from said second gate and said drain.

5. (Original) The fuse of Claim 4, wherein programming is effectuated by providing a ground reference to said source, the transistor threshold voltage to said first gate, and a program voltage to said drain region and said isolated well region.

6. (Original) The fuse of Claim 5, wherein said program voltage is less than the transistor junction breakdown.

7. (Original) The fuse of Claim 5, wherein reading is effectuated by providing a reference voltage to said first gate and detecting current flow between said source region and said drain region, wherein a programmed state is determined when no current is detected and a non-programmed state is determined when current is detected.

8. (Original) The fuse of Claim 7, wherein said reference voltage is greater than the transistor threshold voltage.

9. (Original) The fuse of Claim 5, wherein reprogramming is effectuated by providing the inverse of said programming voltage to said first gate.

10. (Currently Amended) A programmable fuse cell having a substrate of semiconductor material of a first conductivity type, a source region and drain region disposed in said substrate and spaced apart to define a substantially continuous channel region of monolithic substrate material therebetween, and a layer of insulating material having a uniform thickness and disposed over said source region, drain region and channel region, said transistor fuse comprising:

a transistor fuse comprising:

a first gate and a second gate disposed in a single layer of polysilicon over said insulating material, said first gate disposed overlapping a portion of said source region and said second gate isolated from said first gate and disposed overlapping a portion of said drain region;

said first gate includes a terminal for receiving an externally applied signal and said second gate is capacitively coupled to said drain region; and

a coupling device disposed within said substrate and adapted to increase capacitive coupling of said second gate and said drain region, wherein programming is effectuated by charging said second gate via capacitive coupling with said drain region; and

first circuitry coupled to said first gate terminal and adapted for selecting said transistor fuse for programming via a voltage signal; and

second circuitry coupled with said drain region and said coupling device and adapted for programming and reading the programming state of said transistor fuse.

11. (Previously Presented) The fuse cell of Claim 10, wherein said second circuitry includes a further transistor coupled with said drain region and said coupling device for delivering a programming voltage signal when selected on.

12. (Previously Presented) The fuse cell of Claim 11, wherein said second circuitry includes further circuitry coupled with said transistor fuse for detecting current flow therein when said further transistor is selected off.

13. (Original) The fuse cell of Claim 10, wherein said programming is effectuated via application of a voltage signal to said drain region and said coupling device which is less than junction breakdown of said transistor fuse.

14. (Original) The fuse cell of Claim 10, wherein said transistor fuse further comprises an extended width drain portion integral with said drain region disposed in said substrate overlapping said second gate for increasing capacitive coupling.

15. (Original) The fuse cell of Claim 10, wherein said transistor fuse further comprises an extended width drain portion integral with said drain region disposed in said substrate overlapping a portion of said second gate and a well region disposed in said substrate also overlapping a portion of said second gate, wherein said well region is isolated from said second gate and said drain.

16. (Original) The fuse cell of Claim 10, wherein programming is effectuated by providing a ground reference to said source, the transistor threshold voltage to said first gate via said first circuitry, and a programming voltage to said drain region via said second circuitry.

17. (Original) The fuse cell of Claim 16, wherein said program voltage is less than the transistor junction breakdown.

18. (Original) The fuse cell of Claim 16, wherein reading is effectuated by providing a reference voltage to said first gate via said first circuitry and detecting current flow between said source region and said drain region via said second circuitry, wherein a programmed state is determined when no current is detected and a non-programmed state is determined when current is detected.

19. (Original) The fuse cell of Claim 18, wherein said reference voltage is greater than the transistor threshold voltage.

20. (Previously Presented) The fuse cell of Claim 16, wherein reprogramming is effectuated by providing a voltage of opposite polarity to the programming voltage to said first gate via said first circuitry.

Appl. No.: 10/769,101
Amdt. Dated November 16, 2005
Reply to Office Action Dated September 19, 2005

Amendments to the Drawings

The attached sheets of drawings include formal drawings for Figures 1-7 and reflecting changes to Figure 4 as suggested by the examiner. These sheets, which include Figures 1-7, replace the original sheets including Figures 1-7. In Figure 4, item 410 is illustrated.

REMARKS

Claims 1-20 are pending in the application. Claims 1 and 10 have been amended. Support for the amendments may be found throughout the specification, and particularly at pages 9-11 and Figures 2A, 3A and 4A. No new matter has been added. Applicants respectfully submit that the amendments place the application in a condition for allowance, and request favorable consideration of the application in light of the above amendments and following remarks.

Objections to the Drawings and Claims

The objections to the drawings and claims have been obviated by appropriate amendments. Applicants have attached formal drawings correcting the objections noted by the Examiner.

Rejections Pursuant 35 U.S.C. § 102

Claims 1-3, 10-14, and 16-20 have been rejected under 35 U.S.C. 102(e) as being anticipated by *Hsu, et al.* (US Pat. No. 6,617,637). Claims 1-10 and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by *Wang* (US Pat. No. 5,886,378). Applicants respectfully submit that neither *Hsu* nor *Wang* disclose the limitations of the pending claims.

Independent claim 1 relates to an electrically programmable transistor fuse having, *inter alia,* source and drain regions disposed in a substrate of semiconductor material having a first conductivity type. Independent claim 10 relates to a programmable fuse cell having, *inter alia,* source and drain regions also disposed in a substrate of semiconductor material having a first conductivity type. In the transistor fuse of claim 1 and the programmable fuse cell of claim 10, the source and drain regions are "spaced apart to define a substantially continuous channel region of monolithic substrate material therebetween."

The cited reference to *Hsu,* on the other hand, relates to first and second transistors 101 and 102, where the first transistor 101 has a floating gate 122 and the second transistor 124 has a select gate. (Col. 3, ll. 17-51). A P+ doped region 132 is disposed between the floating gate 122 and the select gate 124 and serially connects the transistors 101 and 102. (Col. 3, ll. 23-25 and

42-44). The P+ doped region 132 is a drain of transistor 101 and also a source for transistor 102. (Col. 3, ll. 47-49). Figures 2a, 2b, and 3 of *Hsu* illustrate that the P+ doped region 132 is located in the channel between P+ doped region 136 and P+ doped region 140. Accordingly, to the extent *Hsu* describes a channel defined by the region between P+ doped region 136 and P+ doped region 140, that channel includes the P+ doped region 136, which serially connects the transistors and acts as a source/drain region for the serially connected transistors 101 and 102.

Likewise, *Wang* relates to an EEPROM device having a gate 156 and floating gate 160 each overlying a P-region between N-regions 136 and 140. (Col. 3, ll. 10-17). Figures 5 and 6 illustrate that the N-region 138 is located in a channel defined between regions 136 and 140. Gate 156 and floating gate 160 both overlay the N-region 138, which is the source for transistor 162 and is "connected to the drain 138 of the first transistor 158." (Col. 3, ll. 17-23). Transistors 156 and 162 are also connected to each other though the connection of N-region 138 between gates 156 and 162. (Col. 3, ll. 42-44). Accordingly, to the extent *Wang* describes a channel defined by the region between N-regions 136 and 140, that channel includes an N-region 138.

Neither *Hsu* nor *Wang* disclose the electrically programmable transistor fuse of claim 1 or the programmable fuse cell of claim 10. Both *Hsu* and *Wang* disclose a non-uniform, disconnected channel region between a source and drain. In particular, in *Hsu* a P+ doped region is located in a channel region defined between P+ doped regions 136 and 140 and in *Wang*, an N-region 138 is located in the channel between N-regions 136 and 140. Because the channel regions include the P+ doped region (*Hsu*) or the N-region (*Wang*), neither channel is continuous. Since the channel regions of *Hsu* and *Wang* include material other than a substrate material, the channels of *Hsu* and *Wang* are not monolithic substrate material. To the contrary, the channel regions of *Hsu* and *Wang* are disconnected and consist of a grouping, or assemblage, of materials. The channel region between the source and drain as recited in claims 1 and 10, on the other hand, is "substantially continuous" and "monolithic." Therefore, the channel regions of claims 1 and 10 is uniform without a P+ doped region of *Hsu* or the N-region of *Wang*. Accordingly, limitations of claims 1 and 10 are entirely missing in the cited art. Applicants respectfully submit that the amendments place claims 1 and 10 in a condition for allowance.

Dependent Claims 2-9 and 11-20

Applicants also respectfully submit that dependent claims 2-9 and 11-20 are not anticipated by the cited art. As discussed, limitations for independent claims 1 and 10 are not disclosed by the cited art. Therefore, the limitations of the claims dependent therefrom are also not disclosed or fairly suggested by the cited combination. Accordingly, Applicants respectfully submit that claims 2-9 and 11-20 are not anticipated.

CONCLUSION

In view of the foregoing, Applicant respectfully requests favorable consideration and allowance for all pending claims. If the examiner believes that a telephone conference would expedite allowance of the application, the examiner is invited to call the undersigned.

Respectfully submitted,

November 16, 2005

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